

PRELIMINARY AMENDMENT

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Title: ASYNCHRONOUSLY-ACCESSIBLE MEMORY DEVICE WITH MODE SELECTION CIRCUITRY FOR BURST OR PIPELINED OPERATION

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Sub 3/15/96
60. (New) A method for accessing a storage device, comprising: (READ)
receiving a first address to the storage device; ROW ADDR
receiving a burst/pipeline signal;
selecting between outputting information from the storage device and inputting new
information to the storage device;
selecting between an asynchronously-accessible burst mode and an asynchronously-accessible pipelined mode of operation of the storage device in response to the burst/pipeline signal;
obtaining a second address to the storage device; and
asynchronously accessing a storage element of the storage device in the selected mode of operation using the first address and the second address.

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61. (New) A method for accessing several different locations in an asynchronously-accessible memory device, comprising:
selecting a pipeline mode of operation;
providing an initial external address associated with asynchronously accessing the COL ADDR
asynchronously-accessible memory device in the pipelined mode of operation;
generating at least one subsequent internal address patterned after the initial external address while in the pipelined mode of operation; COL ADDR
switching modes to a burst mode of operation; and →
providing a new external address for every access associated with asynchronously accessing the asynchronously-accessible memory device while in the burst mode of operation. COL ADDR

62. (New) A method of specifying burst or pipeline access to a memory, comprising:
receiving an external row address; ROW ADDR
receiving a pipeline/burst select signal;
selecting an external address path if the pipeline/burst signal indicates a pipeline mode of operation; and CAS